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10/676,929	09/30/2003	Amit Singh	X-1495 US	7851

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,929	SINGH, AMIT	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *12-17 and 24-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed action

1. This final office action is a response to the amendment and remarks/arguments filed on 01/09/2006.

2. Claims 4,18, and 19 have been amended.

Applicant's remarks/arguments filed on 01/09/2006 have been fully considered but they are not persuasive. Therefore, the rejections based on the prior art of record are retained.

Claims 1-28 are pending.

3. Applicant's election with traverse of claims 1-11 and 18-23 (group I) in the reply filed on 01/09/2006 is acknowledged. However, because applicant did not distinctly and specially point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

4. The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an

application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-3, 7, and 18** are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (US Patent No. 6813754).

Referring to claim 1, Wu et al. disclose a method of physical circuit design comprising the steps of:

packing components of a circuit design that are dependent upon an architecture of the circuit design (Fig. 1C, col. 1, ll. 32-35; *Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

assigning initial locations to components of the circuit design (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13);*

clustering a plurality of components of the circuit design according to design constraints (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*); and placing the components of the circuit design to minimize critical connections (*Fig.4, col. 4, lines 14-56).*

Referring to claim 2, Wu et al. disclose the method of claim 1, wherein said clustering step operates on components that are not dependent upon the architecture of the circuit design (*col. 3, lines 40-45; Wu et al. discloses after a placement (step 206), each CLB may have: unassigned clusters (i.e. the clusters are not depended on a circuit architecture)).*

Referring to claim 3, Wu et al. disclose the method of claim 1, wherein said step of assigning initial locations is not timing driven (*in col. 7, lines 10-17, Wu el al. also*

disclose that the method can be applied to alternative constraints such as power, routing congestion, or routing overlapped).

Referring to claim 7, Wu et al. disclose the method of claim 1, said clustering step further comprising the step of adding a slice to a configurable logic block if the slice has a critical attraction to a slice already included in the configurable logic block (*col. 4, lines 29-56*).

Referring to claim 18, Wu et al. disclose a system (*col. 7, lines 25-45*) for physical circuit design comprising:

means for packing components of a circuit design that are dependent upon an architecture of the circuit design (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

means for assigning initial locations to each component of the circuit design (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

means for clustering the components of the circuit design by combining slices and including slices into configurable logic blocks according to design constraints (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

means for placing the components of the circuit design to minimize critical connections (*Fig.4, col. 4, lines 14-56*);

means for declustering the circuit design *(Fig. 3,col. 4, lines 1-4)*; and

means for performing additional post-placement placer tasks on the declustered circuit design *(Fig. 3,col. 4, lines 1-4)*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 4, 8, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US Patent No. 6813754) in view of Chen et al. (US Patent No. 5475830).

Referring to claim 4 and similarly recited 19, Wu et al. disclose substantially all the elements in claim 1 except said clustering step further comprising the step of combining slices that share control signals and clock sources to form a combined slice such that the total number of components of the combined slice does not exceed a threshold number of components.

Chen et al. disclose the method of clustering storages instances that share data paths ("control signals") and clock paths ("clock sources") (*col. 2, lines 30-38; Fig. 6, col. 13, lines 58+ to col. 14, lines 1-21; Fig. 11a, col. 14, lines 18-21*) such that each cluster should include a number of components no larger than the threshold size which can be handle by a programmable circuit device (*col. 14, lines 28-30*)

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Chen et al. to thereby for the number of combined components (or slice) including in a cluster does not exceed the maximum number of components which the cluster can handle (*col. 14, lines 28-30*).

Referring to claim 8, **Wu et al**. disclose substantially the method of claim 1, except

said clustering step further comprising the step of using fanout to determine which slice is included in a configurable logic block if more than one slice to be added to the configurable logic block has an equivalent critical attraction to a slice within the configurable logic block.

Chen et al. disclose the step of using the criteria of the most fanout of a net that connects between components to determine which component in an oversized cluster to be selected into a smaller cluster (*col. 14, lines 28-44*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Chen et al. to thereby for the number of combined components (or slice) including in a cluster does not exceed the maximum number of components which the cluster can handle (*col. 14, lines 28-30*).

8. **Claims 5, 9, 10, 20, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu et al**. (US Patent No. 6813754) in view of **Russo et al**. entitled

"A computer-based-design approach to partitioning and mapping of computer logic graphs" (Proceedings of the IEEE Volume 60, Issue 1, Jan. 1972 Page(s): 28 – 34).

Referring to claim 5 and similarly recited 20, **Wu et al**. disclose substantially the method of claim 1, further comprising:

declustering the circuit design (*Fig. 3, col. 4, lines 1-4*); and

performing post-placement tasks on the declustered circuit design (*Fig. 3, col. 4, lines 1-4*); and

However, **Wu et al.** do not disclose wherein said clustering step further comprising including slices in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs.

Russo et al. disclose a partitioning (or "clustering") and mapping of logic blocks wherein one constraint required for a partition of logic blocks to be acceptable is that a total number of external connections (or I/O pins) should be equal or less than (or " not exceed") an external connection capacity (or " a threshold number of inputs and outputs") (*see Fig. 1; page 28*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Russo et al. to thereby for satisfying a design constraint on the pin capacity of configurable logic blocks (*page 28*).

Referring to claim 9 and similarly recited claim 22, Wu et al. disclose substantially the method of claim 1, said clustering step further comprising the steps of:

(a) selecting a critical connection of the circuit design (*Fig. 4; col. 4, lines 29-62*);

(b) identifying a first slice connected to the critical connection (*Fig. 4; col. 4, lines 29-62);*

(c) if the first slice is not clustered, identifying a second slice having a most critical attraction to the first slice (*Fig. 4, col.4, lines 29-62*);

(e) repeating steps (a), (b), (c), and (d) for further slices connected to the critical connection (*Fig. 4, col.4, lines 29-62*).

However, **Wu et al**. do not disclose the step (d) including the second slice with the first slice in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs; and

Russo et al. disclose a partitioning (or "clustering") and mapping of logic blocks wherein one constraint required for a partition of logic blocks to be acceptable is that a total number of external connections (or I/O pins) should be equal or less than (or " not exceed") an external connection capacity (or " a threshold number of inputs and outputs") (*see Fig. 1; page 28*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Russo et al. to thereby for satisfying a design constraint on the pin capacity of configurable logic blocks (*page 28*).

Referring to claim 10, Wu et al. disclose the method of claim 9, further comprising the step of repeating said steps (a)-(e) for further critical connections (*Fig. 4, col.4, lines 29-62*).

Allowable Subject Matter

9. **Claims 6, 11, 21, and 23** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. **Claims 6, 11, 21 and 23** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

wherein the threshold number of inputs and outputs is less than the number of inputs and outputs that can physically be accommodated by the configurable logic block so as to leave white space in the configurable logic block for post-placement circuit optimizations.

Response to Remarks

11. Applicant's arguments are not persuasive. Referring to claims 1 and 18, Applicant stated that Wu does not teach or suggest " clustering a plurality of components of the circuit design according to design constraints." (claim 1). Examiner disagrees with Applicant's argument. Wu does teaches or suggests packing (or clustering) logic cells/ clusters to different blocks corresponding to the design (col. 3, ll. 25-32) which can be a circuit design structure (col. 1, ll. 32-35; Fig. 1C; col. 3, ll. 25-32) or a design constraint, for example a design constraint for optimizing local connectivity between cells and/ or clusters (col. 3, ll. 25-32).

12. Further, Applicant admitted in the related art " non-mandatory packing can include packing components " ("clustering a plurality of components of the circuit design ", in claim 1) "to achieve a particular signal propagation delay based up on topological circuit information." (" according to design constraints.", in claim 1). (See application specification, paragraphs [0004]-[0005]).

13. As detailed above, Wu does teach or suggest each and every element of Applicant's claim 1 and similarly recited claim 18. Claims 2-11 and 18-23 depend from the rejected claims 1 and 18.

Conclusion

14. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free)

Tuyen To

Examiner

Art Unit 2825

VUTHE SIEK
PRIMARY EXAMINER